INVITED PAPER *Special Section on Analog Circuit Techniques and Related Topics*

# How the Author's Group Came Up with Ideas in Analog/Mixed-Signal Circuit and System Area

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**SUMMARY** This article reviews the author's group research achievements in analog/mixed-signal circuit and system area with introduction of how they came up with the ideas. Analog/mixed-signal circuits and systems have to be designed as well-balanced in many aspects, and coming up ideas needs some experiences and discussions with researchers. It is also heavily dependent on researchers. Here, the author's group own experiences are presented as well as their research motivations.

***key words:*** *circuit and system research, waveform sampling, ADC, DAC, TDC, analog IC test*

## 1. Introduction

This article reviews the author's group research achievements in analog/mixed-signal (AMS) circuit and system area with introduction of how they came up with the ideas as well as the research motivations. Many of their approaches are based on signal processing algorithms, control theory and mathematics, which are different from other AMS IC design researchers, though their practical industry applications are taken into account in many cases. AMS circuits and systems have to be designed as well-balanced in many aspects, and design trade-off is an important concept. Coming up ideas needs some experiences and discussions with researchers both in academia and industry. It is also heavily dependent on researchers themselves. Here, the author's group own experiences are presented as well as their research motivations [1]–[7].

In Sect. 2, circuits related to resistor and capacitor networks are shown. In Sects. 3, 4, waveform sampling technologies and Nyquist-rate DACs are introduced respectively. In Sects. 5, 6, 7, successive-approximation-register (SAR) ADCs with redundancy, time-interleaved ADCs, and time-to-digital converters (TDCs) are described. In Sects. 8, 9, ΔΣ ADC/DAC/TDC and dynamic element matching techniques are shown, while in Sect. 10, other research results are summarized. Section 11 concludes the paper.

All of the cited references in this paper are from the author's group and for the technical details, the reader can refer to them.

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## 2. Resistor and Capacitor Networks

### 2.1 Spatial and Temporal Dynamics of Active Resistor Network

A long time ago, the author was involved in the research for an analog image processing neuro-chip or vision chip which consisted of positive and negative resistors (i.e., active resistors) (Fig. 1) [8]–[10], and the following circuit theorem was derived [11], [12]:

*"For uniform active networks, the spatial and temporal stability conditions are equivalent."*

Its generalization to non-uniform networks is discussed in [13], [14].

Triggered by this research, the author became interested in the resistor network, and his group were involved in extension and non-ideality analysis of R-2R ladder DAC and Hopfield network. Also, the research for the circulant active resistor network dynamics in [12] leads to the RC polyphase filter because it has the circulant structure.

### 2.2 General Resistor Network DAC

We have performed design and analysis of DACs based on the non-uniform current division resistive ladder, and came up with a new configuration DAC with segmentation of binary, quaternary and unary resistive-ladders, which enables two times gain with equivalent chip area and current sources to the conventional DAC (Fig. 2). Also, our simulation showed that the DNL deviation of the proposed one is a little better than the conventional one [15], [16].

Further, we investigated a systematic configuration method of resistor ladder networks for N-ary DACs, by generalizing the configuration of the conventional R-2R DAC [17].

Notice that the capacitor-type DAC is popular due to low power, but still the resistor-type DAC is advantageous

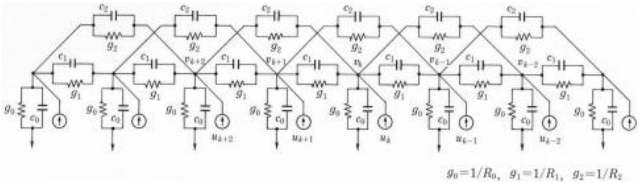


**Fig. 1** Active resistor network with positive and negative resistors [9].

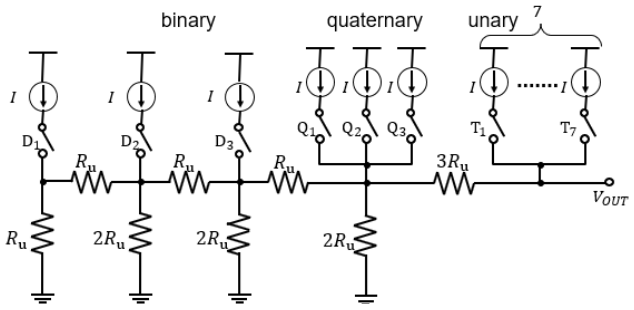



**Fig. 2** Proposed resistor ladder DAC with binary, quaternary and unary combination [15] ©IEEE.

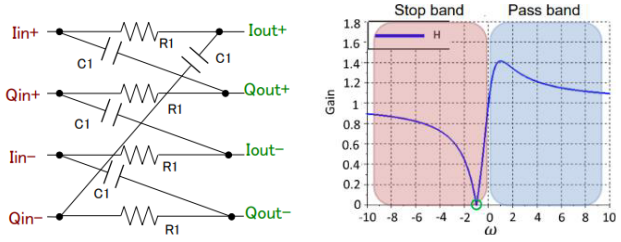



**Fig. 3** First-order RC polyphase network (left) and its gain characteristics (right) [20] ©IEEE.

in some applications, such as programmable DC voltage generator thanks to no requirement for switching.

### 2.3 RC Polyphase Filter and Hilbert Filter

About 20 years ago, the author heard a presentation from Katholieke Universiteit Leuven group at ISSCC; there an RC polyphase filter and its curious behavior were shown. Then he analyzed it using complex signal processing and circulant matrix theories [7], [18], [19].

After several years, an adjunct professor of Gunma University introduced a digital Hilbert filter at his class, and then the author had an intuition that the RC polyphase filter has characteristics as a complex analog Hilbert filter. We found that phase characteristics of the RC polyphase filter have the same as those of the Hilbert filter. Also, its gain characteristics can be approximated as the Hilbert filter; as its order becomes higher, its gain characteristics become closer to the ideal Hilbert filter (Fig. 3) [20].

As far as the author investigated, the RC polyphase filter can be the best approximated to the Hilbert filter, compared to other complex analog filters.

### 2.4 Explicit Transfer Function Derivation of High-Order RC Polyphase Filter

The direct derivation of the transfer function of a high-order RC polyphase filter is very complicated with hand calculation. However, one of Ph.D. course students did it relatively easily [21], [22]. Its point is to denote internal node voltages V, $jV$, $-V$, $-jV$ instead of $V_{I+}$, $V_{Q+}$, $V_{I-}$, $V_{Q-}$ in general form (Fig. 4).

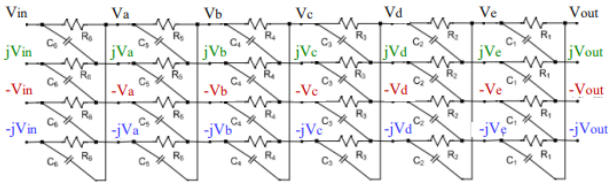



**Fig. 4** High-order RC polyphase network [21] ©IEEE.

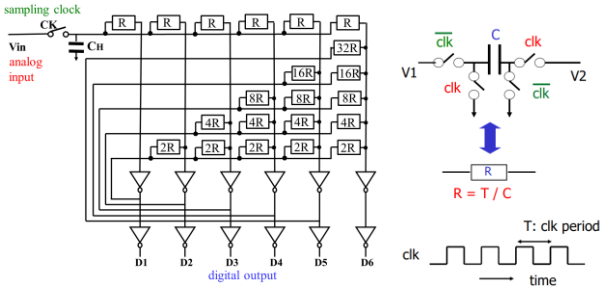



**Fig. 5** Asymmetric Hopfield network with resistors (left) and switched capacitor circuit (right) [23].

### 2.5 Resistor and Capacitor Hopfield Network Asynchronous SAR ADCs

The Hopfield network was proposed a long time ago, but it has not been widely used in practice. On the other hand, recently an asynchronous SAR ADC becomes popular. These motivated us to revisit the Hopfield network. Then we came up with an asynchronous SAR ADC with parallel comparators and switched capacitor configuration based on asymmetric Hopfield network [23]. In principle, the original asymmetric Hopfield resistor network can realize an ADC. However, it requires many resistors with giga or even tera-order Ω. Hence, we investigated to replace the huge resistors with switched capacitor circuits (Fig. 5).

The proposed N-bit SAR ADC uses N comparators operating in parallel and asynchronously without SAR logic and an internal high-frequency clock. Each lower-bit comparator can operate by look-ahead of its higher-bit comparator results for high speed, and its AD conversion latency is only one or two clock cycles.

## 3. Waveform Sampling Technologies

The author was involved in the research for wideband measurement and test systems, and his group investigated wideband waveform sampling technologies (Fig. 6). In this section, their research results are introduced [1].

### 3.1 Residue Sampling

ADC and DAC are considered as division and multiplication operations. On the other hand, waveform sampling causes spectrum folding which is similar to but different from division operation in frequency domain.

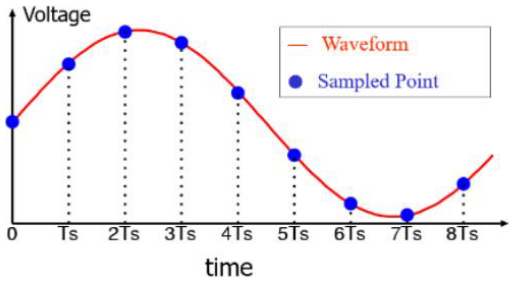



**Fig. 6** Waveform sampling.

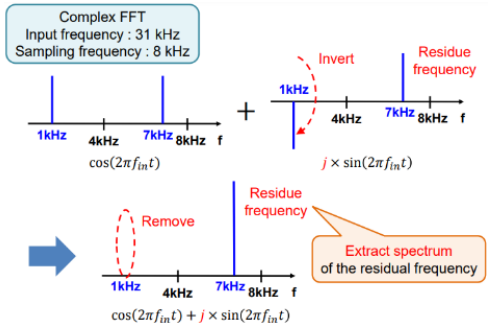



**Fig. 7** Residue frequency generation for complex signal cos(2πt) + j sin(2πt) using sampling [25] ©IEEE.

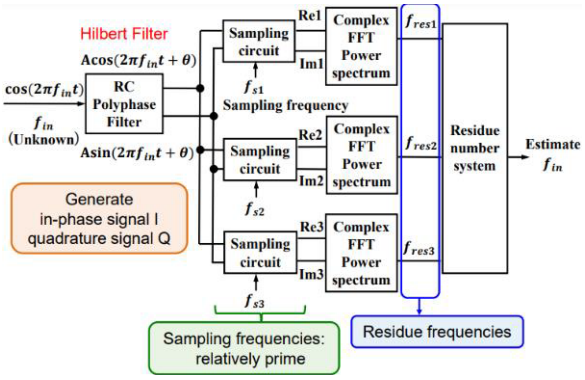



**Fig. 8** Residue sampling system [25] ©IEEE.

The author's group found that sampling of a complex sinusoidal signal ("cosine + j sine" signal) can realize "frequency division" operation (Fig. 7), and we came up with a high-frequency signal estimation circuit using multiple low-frequency sampling circuits following an analog Hilbert filter (RC polyphase filter) and ADCs (Fig. 8) [24], [25]; here the sampling frequencies are relatively prime.

A sinusoidal signal with high frequency is provided as an input signal. Then cosine and sine signals with the same frequency are generated with an analog Hilbert filter and they are fed into sampling circuits with different and low sampling frequencies. Their analog outputs are AD converted and for their digital outputs, complex FFTs are performed. The input signal frequency can be estimated from the residue frequencies and the residue number theory: the property of one-to-one mapping between the original number and its

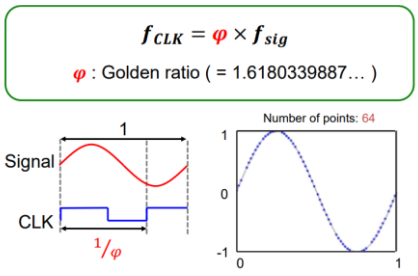



**Fig. 9** Golden ratio sampling and uniform distribution of its sampling points [28] ©IEEE.

residue numbers obtained by division of relatively prime numbers are the key.

The frequency estimation resolution becomes finer as the number of FFT data is increased. Also, we investigated its application to AMS IC testing by collaborating with an automatic test equipment (ATE) manufacturer [26].

### 3.2 Golden Ratio and Metallic Ratio Sampling

The author learned "waveform missing phenomena" in equivalent-time sampling systems, such as sampling oscilloscopes. Then he tried to find the efficient waveform acquisition condition of the relationship between the sampling clock frequency and the sinusoidal input frequency, which does not cause the phenomena. One of his students found by extensive simulations that the golden ratio (1.6180..) is the most efficient for avoiding the waveform missing phenomena (Fig. 9), and we analyzed its effectiveness in theory and simulation [27].

As its extension, we investigated metallic ratio sampling of the sampling frequency and the input frequency, which also realizes efficient waveform acquisition. Further several interesting properties of the metallic ratio sampling in the view point of the integer theory were found [28].

These results can be utilized in several LSI testing applications such as ADC histogram test [29] because there the sampling clock and the input signal can be controlled intentionally. Also, the golden ratio and metallic ratio sampling techniques can be used for pseudo random signal generation targeted for Monte Carlo simulations [30].

### 3.3 Non-Ideality Analysis of Waveform Sampling

Sampling jitter is a serious problem for wideband waveform acquisition (Fig. 10), and high-frequency electronic measurement instrument companies are interested in this issue. Our study on the jitter effect was motivated to realize a high-speed track-hold circuit such as in [31].

Exact noise power ($P_j$) and SNR degradation due to sampling jitter are derived in Eqs. (1), (2) assuming that the jitter (εn) follows the Gaussian distribution of N (0, $\sigma_j$) and the input is a sinusoidal signal of a frequency $f_{in}$ [32], [33].

$$P_j = A^2 \left[1 - \exp\left(-2\pi^2 f_{in}^2 \sigma_j^2\right)\right] \quad (1)$$

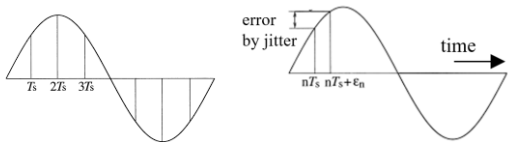



**Fig. 10** Jitter effects to waveform sampling [33].

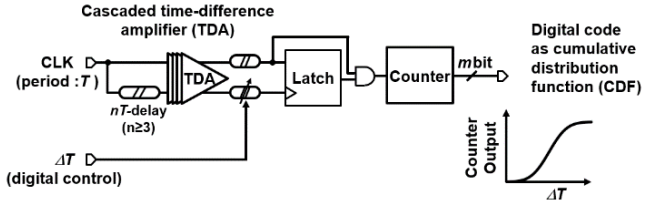



**Fig. 11** Jitter measurement circuit [36] ©IEEE.

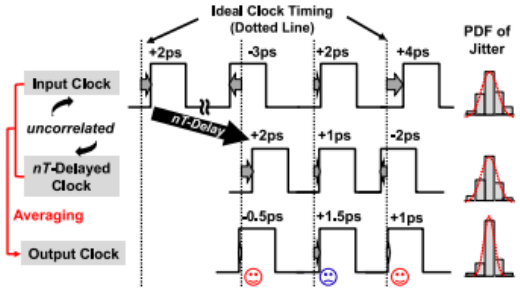



**Fig. 12** Conceptual image of the proposed clock jitter reduction circuit using a phase averaging between uncorrelated self-delayed clock edges [38].

$$SNR = -10\log 2\left[1-\exp\left(-2\pi^2 f_{in}^2\sigma_j^2\right)\right] \quad [\text{dB}]. \tag{2}$$

It was impressive that the third author of [33] knew and used the following formulae (3), (4) for derivation of Eqs. (1), (2):

$$E\left[\cos\left(\omega\varepsilon_n\right)\right] = \exp\left(-\frac{\omega^2\sigma_j^2}{2}\right) \tag{3}$$

$$E\left[\sin\left(\omega\varepsilon_n\right)\right] = 0. \tag{4}$$

Notice that in actual sampling circuit, jitter distribution is often not Gaussian.

It is widely believed that sampling jitter effect is the fundamental limitation of the ADC performance. But the author considers that the continuous-time ΔΣ ADC can overcome this problem; jitter effects for internal ADC are noise-shaped and those for internal DAC can be reduced by jitter insensitive DAC design (such as RF DAC) [34], [35].

Our jitter measurement circuit and jitter reduction circuit are shown in Figs. 11, 12 respectively [36]–[38], developed by their first author.

Further we investigated input-dependent sampling-time error effects in MOS samplers [39] and finite aperture time affects in sampling circuit (Fig. 13) [40] as well as timing error effects for DAC [41] and CMOS ADC nonlinear input capacitance for input differential amplifier array [42]; these were done to understand the AMS circuits and systems well.

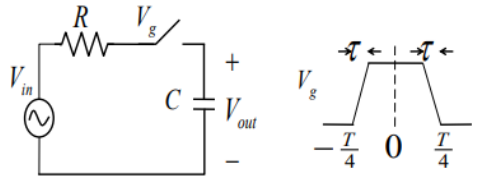



**Fig. 13** Sampling circuit with aperture time τ [40] ©IEEE.

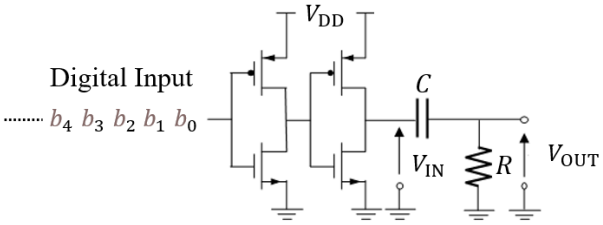



**Fig. 14** Relaxation DAC with HPF [43].

## 4. Nyquist-Rate DAC

### 4.1 Relaxation DAC with HPF

The author considers that differentiation or high-pass filter is interesting. Also, he taught two's complement in his basic circuit course. Then he came up with HPF usage for a relaxation DAC (ReDAC) (Fig. 14) and found that it produces with positive and negative polarity output for digital input in two's complement format [43]. The proposed ReDAC with HPF is an extension of the original ReDAC using LPF which generates an analog output with only positive polarity.

### 4.2 Gray-Code Input DAC

When the author started to study ADC design, he realized that Gray-code is frequently used there because it is robust compared to the binary code. Gray code is a binary numeral system where two successive values differ in only one bit, and the conversion between binary-code and Gray-code can be easily realized by XOR circuits (Table 1).

Then he wondered why it is not used for DAC; if it is used, the glitch can be reduced. DAC glitch is a serious problem such as in graphic display applications. He asked the authority of ADC/DAC design, who answered that the Gray-code input DAC configuration had not been invented even though many researchers tried.

The author taught at his circuit class that Gray code and binary code are converted using EXOR logic. Then his group came up with three types of Gray code input DACs (current-steering, charge-mode and voltage-mode DACs) which use analog switch matrices equivalent to EXOR (Fig. 15) [44].

### 4.3 DAC Architectures Based on Number Theory

Integers have many interesting properties such as polygonal number theorem and Goldbach conjecture of prime numbers, and we considered to use these for new DAC architectures

**Table 1** Binary code and Gray code.

| Decimal Number | Binary Code | Gray Code |
|---|---|---|
| 0 | 0000 | 0000 |
| 1 | 0001 | 0001 |
| 2 | 0010 | 0011 |
| 3 | 0011 | 0010 |
| 4 | 0100 | 0110 |
| 5 | 0101 | 0111 |
| 6 | 0110 | 0101 |
| 7 | 0111 | 0100 |
| 8 | 1000 | 1100 |
| 9 | 1001 | 1101 |
| 10 | 1010 | 1111 |
| 11 | 1011 | 1110 |
| 12 | 1100 | 1010 |
| 13 | 1101 | 1011 |
| 14 | 1110 | 1001 |
| 15 | 1111 | 1000 |

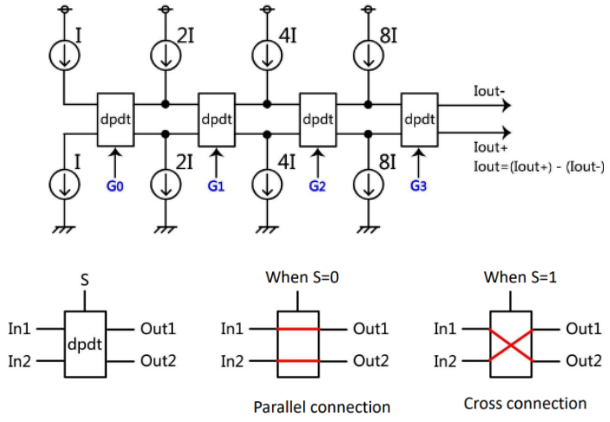



**Fig. 15** Gray-code input current-mode DAC [44] ©IEEE.

as curiosity-driven university research: polygonal number DAC and prime number DAC [45]. We showed that each consists of a few current sources, a resistor network, switch arrays and a decoder circuit. Properties of these DACs are positioned between binary and unary DAC ones.

### 4.4 DAC Linearity Improvement Algorithm with Unit Cell Sorting Based on Magic Square

The author enjoyed introductory mathematical books which describe about Magic Square (Fig. 16), Latin Square and Knight Tour. These were intellectually interesting but their effective applications were not found. Then he considered whether they can be applied to AMS IC design; this is curiosity-driven research. We proposed to use Magic Square, Latin Square and Euler Knight Tour as unit cell selection order algorithms of 2D pseudo random number sequences to cancel systematic mismatch effects among unit cells of a unary DAC and improve its linearity (Fig. 17) [46]–[48].

We also investigated an algorithm called 3-stage current sorting in half-unary weighted current cells to improve the linearity of a current-steering DAC [49].

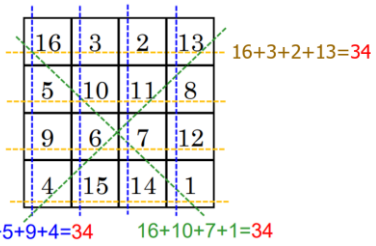



**Fig. 16** 4 × 4 Magic square and its constant sum characteristics.

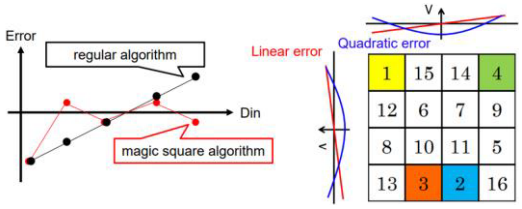



**Fig. 17** Magic square layout of unit cells for a unary DAC which cancels their linear/quadratic gradient errors.

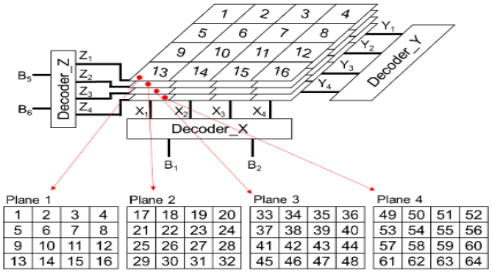



**Fig. 18** X, Y, Z-decoders and unit cells with virtual 3D layout for 6-bit unary DAC [50].

### 4.5 Unit Cell Mismatch Scrambling Method for High-Resolution Unary DAC Based on Virtual 3D Layout

We proposed a unit cell mismatch scrambling method for a high-resolution unary DAC based on virtual 3D layout, to improve its Spurious Free Dynamic Range (SFDR) [50]. This can be implemented with simple interconnections and scrambling circuits, compared to that based on the 2D layout.

It is to care for the static characteristics mismatches using the Dynamic Element Matching (DEM) for the unary DAC. We consider here the signal bandwidth of the DAC is from DC to half of the sampling frequency or higher frequency, so that the DEM technique only needs to spread the spectrum of the spurious tones caused by the mismatches in the entire signal band uniformly without need for mismatch shaping; this is called as mismatch scrambling. However, direct implementation circuit of such mismatch scrambling for the high-resolution unary DAC becomes complicated. We investigated a more hardware efficient method by considering a virtual 3D case, considering X-, Y- and Z-decoders (Fig. 18).

The author came up with this idea from magic cube (or 3D magic square) and an intuition that logic of binary-to-

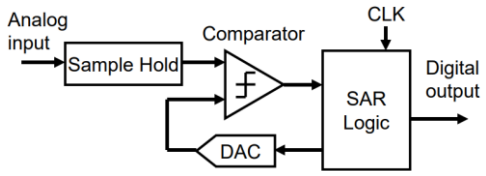



**Fig. 19** SAR ADC configuration [51].

thermometer decoder circuit has some regularity.

## 5. Successive Approximation Register Analog-to-Digital Converter (SAR ADC)

We considered that some redundancy of the SAR ADC (Fig. 19) can relax the requirements for its internal component requirements; there the error is corrected digitally without its measurement. Then the overall performance of the circuit can be improved. The redundancy can be classified into two categories:

(i) Operation redundancy (temporal redundancy): If operation, such as number of SAR steps has some redundancy, the overall AD conversion time can be reduced as well as its reliability is improved.

(ii) Circuit redundancy (spatial redundancy): If redundant hardware, such as multiple SAR comparators is used in an SAR ADC, its overall conversion time can be smaller.

We have investigated both of them. It would be interesting that quantum computer needs redundancy and error correction.

### 5.1 General SAR ADC Algorithm with Operation Redundancy and Digital Error Correction

We generalized the algorithm for SAR ADCs with overlapping steps that allow comparison decision errors (due to, such as DAC incomplete settling and sample-hold circuit incomplete settling) to be digitally corrected [51]. We generalized this non-binary search algorithm, and clarified which decision errors can be digitally correct. The algorithm requires more SAR ADC conversion steps than a binary search algorithm, but the sampling speed of an SAR ADC using this algorithm can be faster than that of a binary-search SAR ADC; this is because the latter must wait for the settling time of the DAC and the sample-hold circuit inside the SAR ADC.

### 5.2 Fibonacci-Sequence Weighted SAR ADC

The author learned from an introductory number theory book that a Fibonacci sequence has many interesting properties and even now new ones are being found. It is widely applied successfully to many areas. Then we considered to apply it to an operation redundancy SAR ADC algorithm. The Fibonacci sequence is defined as follows:

Fibonacci sequence weighted SAR approximates the redundant SAR ADC of the radix 1.6 with integer weights,

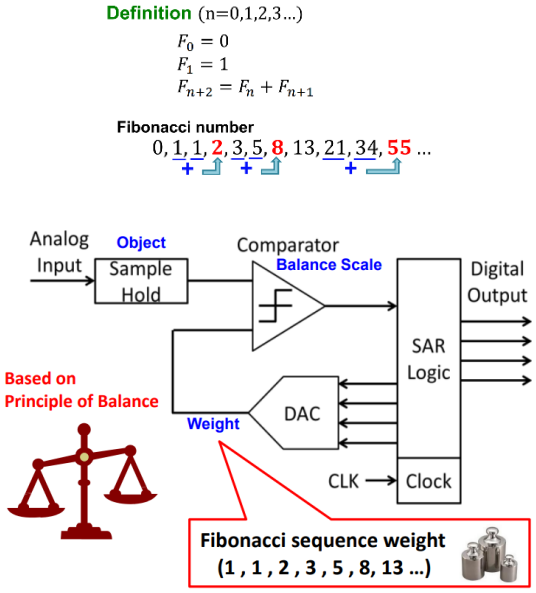



**Fig. 20** Fibonacci-sequence weighed SAR ADC.

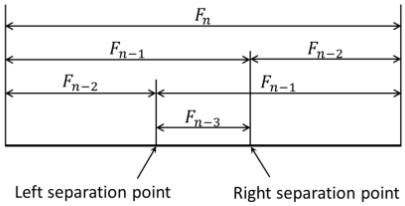



**Fig. 21** Explanation of Fibonacci section search ($F$k: $k$-th Fibonacci number) [54] ©IEEE.

using digital error correction (Fig. 20). Then we found that it is well balanced and fast operation configuration when the settling time of the internal DAC is taken care of. The beautiful characteristics of its "error correction range" were shown. Also, several related results were found [52], [53].

### 5.3 Fibonacci Sequence Weighted SAR ADC as Fibonacci Section Search

The author learned the Fibonacci section search algorithm (Fig. 21) and had an intuition that this is related to the Fibonacci sequence weighted SAR ADC. The Fibonacci section search algorithm is used for finding effectively the extreme value of the unimodal function. Then we found the equivalence between the Fibonacci sequence weighted SAR ADC and the SAR ADC based on the Fibonacci section search algorithm using the unimodal function obtained by the absolute value of the difference between the ADC input voltage and the internal DAC output [54].

### 5.4 Fibonacci Sequence Weighted DAC

We came up with also Fibonacci sequence weighted DAC using R-R resistor networks (Fig. 22) [55]; their termination resistors are important. This can be used inside the Fibonacci

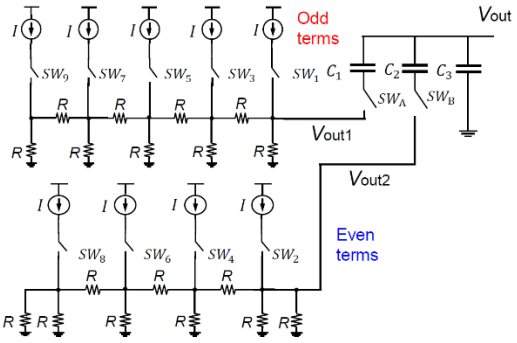



**Fig. 22** Fibonacci-sequence weighted DAC [55] ©IEEE.

sequence weighted SAR ADC.

### 5.5 Pseudo Silver Ratio Weighted SAR ADC

It is well known that when the binary number is 1-bit left-shifted, it is equivalent to multiplication by 2. It is interesting that when it is represented with radix of $\sqrt{2}$, 2-bit left-shift is equivalent to multiplication by 2 and 1-bit left-shift is to multiplication by $\sqrt{2}$.

The sliver ratio ($\sqrt{2}$) is popular especially in Japanese cultures and one of the students considered the (pseudo) silver ratio weighted SAR ADC and found: this method can realize high speed SAR AD conversion when taking account into the internal DAC incomplete settling and using two internal clocks of different periods [56].

Notice that the pseudo silver ratio SA weights are given by

$$1, 1, 1, 2, 2, 4, 4, 8, 8, 16, 16, 32, 32, 64, 64, 128, 128, \ldots,$$

while the binary ones are

$$1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, \ldots$$

### 5.6 Binary SAR ADC with Three Comparators and Digital Error Correction

One of research associates invented an SAR ADC algorithm using three comparators operating in parallel, instead of just one as in conventional SAR ADCs (Fig. 23) [57]–[59]; this is classified into the circuit redundancy SAR ADC. This comparator redundancy enables higher resolution, potentially faster operation, higher reliability and comparator-error correction. We investigated and derived its error-correction algorithm.

### 5.7 Non-Binary SAR ADC Algorithm with Two or Three Comparators

We investigated the design method of an SAR ADC with redundant circuit (two or three comparators) and redundant number of steps, together with digital error correction [60], [61]. Their error correction ranges were clarified. This is the

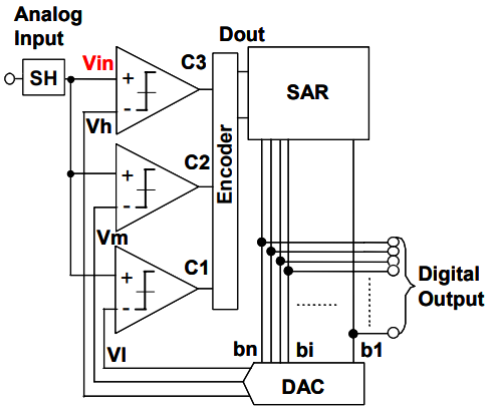



**Fig. 23** SAR ADC with three comparators [57].

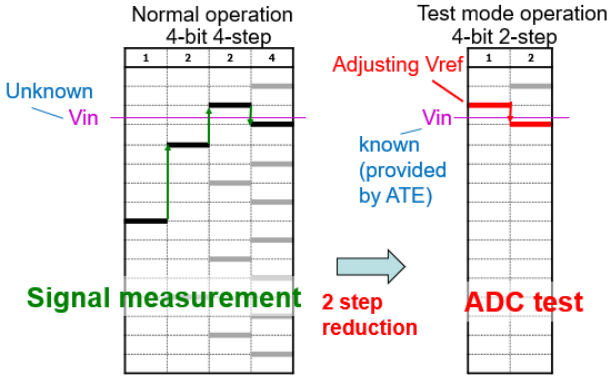



**Fig. 24** Operation of SAR ADC with DFT; number of SA steps can be reduced from 4 to 2 in DC linearity test mode by preadjusting the reference voltage corresponding to the known value of the analog input Vin [62].

generalization of our previous SAR ADC with 3 comparators but without step redundancy and the one with redundant number of steps using one comparator.

### 5.8 Design for Testability That Reduces Linearity Testing Time of SAR ADCs

We developed an SAR ADC chip whose SA weights and number of steps are programmable [62]. As its application we came up with design-for-testability (DFT) of SAR ADC that significantly reduces the testing time of its DC linearity with the ramp input signal (Fig. 24). There are only a limited number of successful ADC DFTs, and this is our trial.

**Remarks:**

(i) Other testing related technologies of the SAR ADC with redundancy are discussed in [63], [64].
(ii) Non-binary two-comparator charge-sharing SAR ADC with digital compensation for comparator offset effects is shown in [65].
(iii) We should notice that single-comparator SAR ADC with operation redundancy increases the number of steps so that the dynamic power consumption increases compared to the binary one without redundancy.

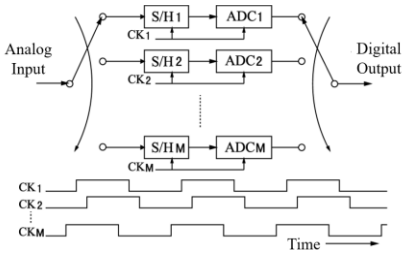



**Fig. 25** Time-interleaved ADC [66] ©IEEE.

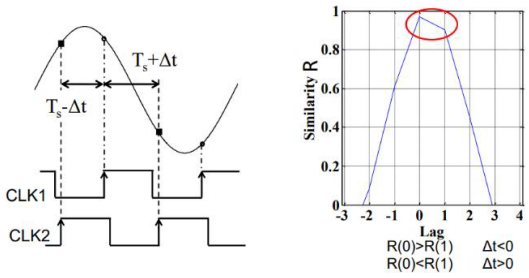



**Fig. 26** Cross-correlation for timing skew detection in two-channel interleaved ADC [70] ©IEEE.

## 6. Time-Interleaved ADC

### 6.1 Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems

The author was involved in an ultra-high-speed ADC research project and reviewed several related papers in Hewlett Packard Journals; one of them was about time-interleaved ADC issues, which inspired him a lot.

A time-interleaved ADC system is an effective way to implement a high-sampling-rate ADC with relatively slow circuits (Fig. 25). In the system, several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate. However, mismatches such as offset, gain, bandwidth mismatches among channel ADCs as well as timing skew of the clocks distributed to them degrade SNDR of the ADC system as a whole. We analyzed their effects in time and frequency domains [66].

**Remarks:**

(i) Linearity mismatch issues are described in [67], [68].
(ii) Notice that the time-interleaved ADC architecture is used for low-power in consumer electronics as well as high-speed-sampling in measurement instruments.
(iii) We investigated a bandwidth-interleaved DAC [69].
(iv) We learned that multi-path (such as time-interleaved, bandwidth interleaved and I, Q-path) and multi sampling clocks in AMS circuits have mismatch problems.

### 6.2 Digital Compensation Method for Timing Mismatches in Time-Interleaved ADC

The most serious mismatch effect for a wideband time-interleaved ADC is the timing skew among channel ADCs. Many compensation methods for it have been proposed which have their own advantages and disadvantages. We targeted for ATE system applications and there its digital calibration is desirable instead of analog one. Then we came up with combining correlation method and fine-delay digital filter for its calibration (Fig. 26) [70].

We use cross-correlation among channel ADC outputs to detect channel timing skew, and do successive-approximation timing adjustments using our proposed linear-phase-digital delay filter to compensate for the timing skew.

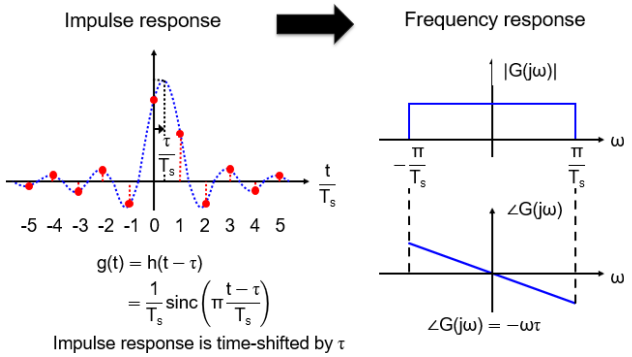



**Fig. 27** Sampling timing shift can maintain the linear phase characteristics. Impulse response, and gain, phase [71] ©IEEE.

It was found that using multi-tone input signals with cross-correlation of outputs provided a more robust way of detecting timing skew than using a single tone.

### 6.3 Digital Filter for Fine Time Delay

We came up with the idea of an FIR digital filter for fine time delay adjustment, by considering the *sinc* function sampling in time domain (Fig. 27). Our digital filter can set its group delay with the arbitrary fine time resolution while it maintains the linear phase characteristics [71], [72]; this can be used such as for the timing skew adjustment of the time-interleaved ADC sampling clocks described above.

## 7. Time-to-Digital Converter (TDC)

Time domain analog circuits such as TDCs are now popular at international conferences in AMS circuit and system area. However, notice that handling the circuit dynamics (timing, bandwidth, slew-rate) is often difficult and troublesome, compared to the voltage signal handling circuit. Also notice that TDCs have been used especially in ATE systems for timing measurement in practice.

### 7.1 SAR TDC with Trigger Circuit

There are many interesting analog circuits for electronic measurement instruments. A long time ago, Tektronix presented a paper about the trigger circuit in an oscilloscope in an international conference on measurement technologies (Fig. 28).

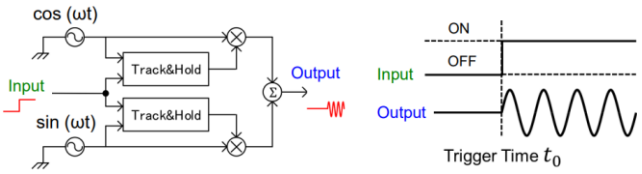



**Fig. 28** Trigger circuit [73] ©IEEE.

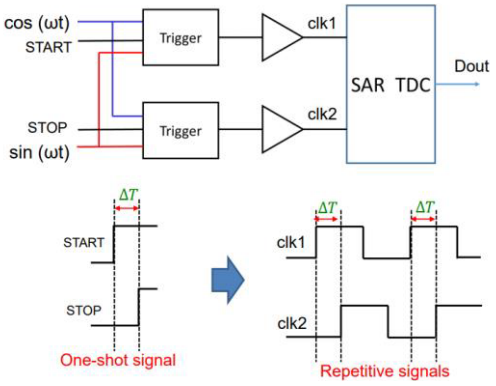



**Fig. 29** SAR TDC with trigger circuits [73] ©IEEE.

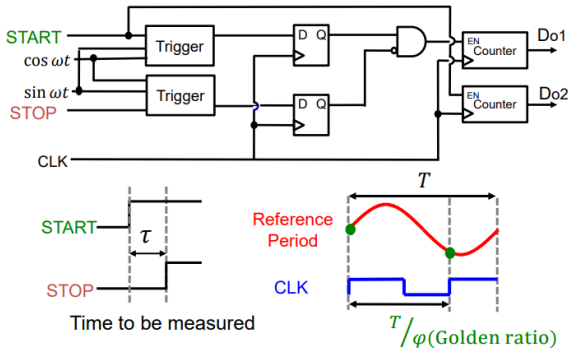



**Fig. 30** Integral-type TDC with trigger circuits [74] ©IEEE.

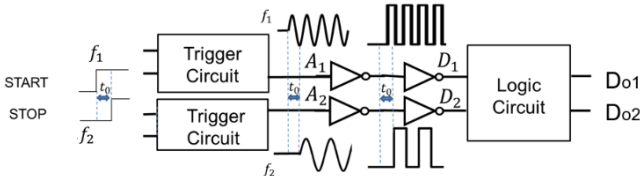



**Fig. 31** Analog centric TDC using two oscillators with different frequencies [76] ©IEEE.

Then later, a TDC became popular and the author came up with its application to an SAR TDC (Fig. 29).

Using the trigger circuits, the rising-edge timing difference between two input timing signals can be held. This enables the SAR TDC to measure the timing when two timing inputs are single-shot as well as repetitive two clocks [73].

It was pointed out at an international conference that an oscillator consumes some amount of power. However, for multi-channel usage of TDCs, it can be shared among them.

### 7.2 Integral-Type TDC

We came up with an integral-type TDC, inspired by an integral-type ADC (Fig. 30) [74]. It can achieve fine time measurement resolution as its measurement time becomes longer and it does not need delay lines. It employs two counters and a repetitive timing signal with a stable frequency clock as well as external reference sine and cosine signals. The input timing difference is measured by a statistical Monte Carlo method.

We found that the golden-ratio relationship between the reference sine/cosine signal frequency and the sampling clock frequency is desirable [75], [76].

### 7.3 TDC Using Two Oscillators with Different Frequencies

As modification of the integral-type TDC, we came up with TDC architectures using two asynchronous oscillators with different frequencies [76]; each starts oscillation with different frequencies from the rising timing of the corresponding input timing signal. By counting their oscillation start phase difference using digital counters, a highly linear stable TDC can be realized.

We came up with two architectures using this principle: analog centric one and digital centric one. The analog centric one uses oscilloscope trigger circuits and the digital centric one uses ring oscillators. For analog centric one, its operation is stable but two external asynchronous sine signals are required (Fig. 31). For digital centric one, all TDC circuits including the calibration can be implemented with full digital circuit.

### 7.4 Residue Arithmetic TDC and Gray Code TDC

We came up with a TDC architecture with residue arithmetic architecture from the motivation of applying the number theory to the AMS circuit design [77]. It can reduce the hardware and power significantly compared to a flash type TDC while keeping comparable performance. But later it was found that it generates a glitch.

Then we came up with a glitch-free TDC based on Gray code, which is an improved version of the residue arithmetic TDC (Fig. 32) [78]. It also keeps advantages of the residue arithmetic TDC.

### 7.5 Stochastic TDC Architecture

Proactive use of variations leads to fine time resolution TDC with full digital circuit was investigated. The author had some knowledge of both the TDC linearity self-calibration with the histogram method and the stochastic TDC. Then he came up with combining them (Fig. 33), and the invented TDC architecture has the following: (1) Encoder circuit that ensures monotonic characteristics. (2) Self-calibration circuit with the histogram method for linearity improvement. (3) Stochastic architecture for fine time resolution

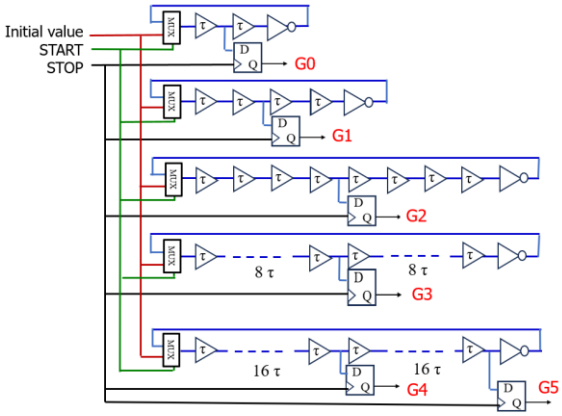



**Fig. 32** Gray-code TDC architecture in 6-bit case [78] ©IEEE.

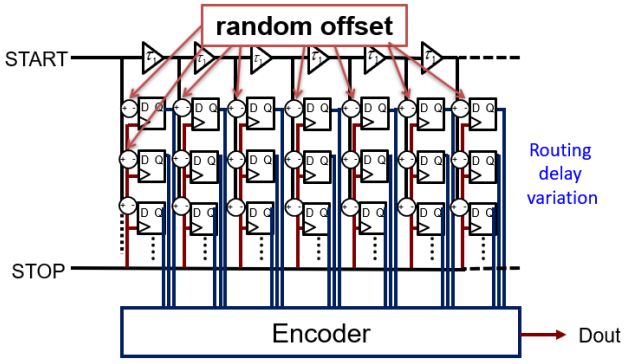



**Fig. 33** Stochastic TDC with linearity self-calibration [79] ©IEEE.

with proactive use of MOSFET characteristics and routing variations [79]–[81].

### 7.6 TDC Linearity Calibration with Metallic Ratio Equivalent-Time Sampling

We implemented a linearity self-calibration TDC with the histogram method using an analog FPGA. This is a foreground calibration, where the normal operation is stopped, the circuit itself measures its own error and then it is compensated by the circuit itself. We performed its experiment, but its linearity accuracy was saturated even if a long calibration time was taken. At that time, its reason was not clear. Later we came up with usage of the metallic ratio sampling, which was successful [82].

### 7.7 ADC Architecture Using TDC

The first author in [83] developed an ADC architecture using TDC for ATE applications (Fig. 34). Since a flash-type TDC is realized with full digital circuits, this ADC can be implemented with mostly digital circuits, which is suitable for fine CMOS implementation. In other words, this ADC performance becomes better as the CMOS technology becomes advanced even though the supply voltage is reduced. This demonstrated that time domain analog signal processing is

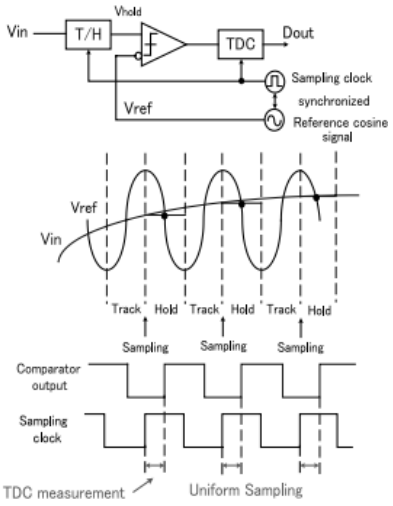



**Fig. 34** Time-domain ADC architecture and its operation. It employs a TDC and performs non-uniform sampling [83].

suitable for fine CMOS technology.

Also note that this ADC performs *non-uniform* sampling because the sampling timing depends on the input voltage value, and digital signal processing to convert *non-uniform* sampling data to *uniform* one is required.

## 8. ΔΣ ADC, DAC, TDC and DC-DC Converter

The author has a strong belief that ΔΣ techniques are applicable to many fields, which always lead to success.

### 8.1 Complex Bandpass ΔΣAD Modulator Without I, Q-Path Crossing Layout and Complex BP DWA Algorithm

We have designed, fabricated and measured a second-order multibit switched-capacitor complex bandpass ΔΣAD modulator which had our new architecture and algorithm [84], [85]. We came up with a complex bandpass filter structure in the forward path with I, Q dynamic matching for the reduction of mismatches between I and Q paths (Fig. 35) [86]. Also we came up with a complex bandpass data-weighted averaging (DWA) algorithm to suppress nonlinearity effects of multibit DACs in complex form to achieve high accuracy (Fig. 36) [87]. The chip employed both of them to evaluate their effectiveness.

### 8.2 Limit Cycle Suppression Technique Using Digital Dither in ΔΣ DA Modulator

We came up with a digital dither technique to suppress limit cycles in a ΔΣ DA modulator [88]. It uses an XOR gate at the modulator output and the digital dither is generated by another ΔΣD modulator. The resolution of the DAC following the modulator is 1-bit (instead of multi-bit) thanks to XOR gate usage, and the overall SNDR does not degrade because the dither is added at the output and hence it is

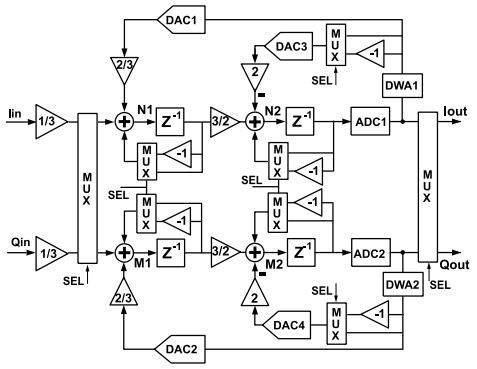



**Fig. 35** Architecture of our complex bandpass ΔΣAD modulator [86].

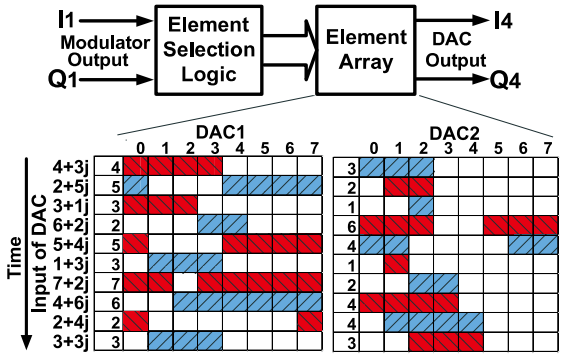



**Fig. 36** Explanation of our complex bandpass DWA algorithm. The unit current cells in the ON state are filled in red for a real part (I-path) and in blue for an imaginary part (Q-path), when the complex input data are sequentially given by 4+3j, 2+5j, 3+j, 6+2j, . . . [87].

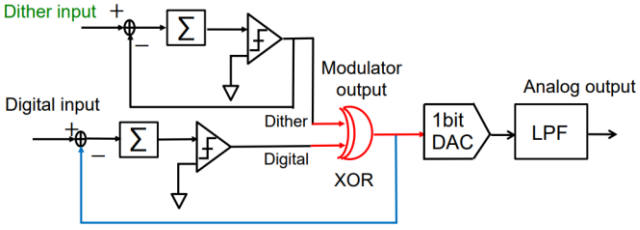



**Fig. 37** ΔΣ DA modulator with digital dither [88].

noise-shaped (Fig. 37). Notice that limit cycles are usually not observed in in a ΔΣ AD modulator due to the device noise inside the AD modulator.

### 8.3 Phase Noise Measurement Techniques Using ΔΣ TDC

It was demanded from industry that short-time testing of phase noise without spectrum analyzer is required at mass-production shipping stage.

Then we came up with a technique for measuring phase noise of a clock using a ΔΣ TDC (Fig. 38) [89]. It can be implemented with simple circuitry, due to the following: (i) Clock under test (CUT) is a repetitive signal. (ii) Time resolution with CUT and reference clock can be finer by using longer measurement time with the ΔΣ TDC. (iii) Phase noise

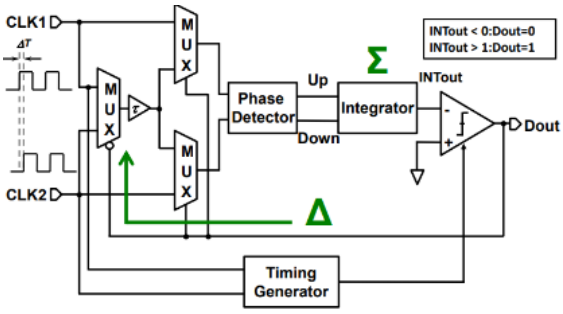



**Fig. 38** ΔΣ TDC configuration [89] ©IEEE.

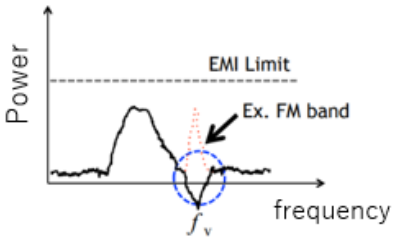



**Fig. 39** Band-select spectrum spread [90].

power spectrum can be calculated from the ΔΣ TDC output data using FFT.

### 8.4 Band-Select Noise Spread Spectrum Clocking

We investigated a ΔΣ TDC and then as its duality, one of students simulated a ΔΣ digital-time converter (DTC). We observed its simulation results in frequency domain and came up with usage as band-select spread spectrum clock for DC-DC converters [90]. This technique can exclude the noise spectrum spread such as in AM, FM radio bands (Fig. 39). Later its several extensions have been investigated by leading of a visiting professor of Gunma University [91].

## 9. Dynamic Element Matching Technologies

It was pointed out by an industry researcher that "multi-bit" usage is mandatory for low-power ΔΣAD modulator, because the operational amplifier slew-rate requirement is significantly relaxed. However, the multi-bit DAC has some nonlinearities in the feedback path, which degrade the overall SNDR of the ΔΣ ADC if no care is taken. Then we investigated several digital signal processing algorithms to suppress the multi-bit DAC nonlinearity effects, which is one of the digitally-assisted analog technologies.

We developed various DWA algorithms:

Muti-BP ΔΣ ADC DWA algorithms [92], Second-order LP DWA algorithms [93], [94], Complex single-BP DWA algorithm [87], Complex multi-BP DWA algorithms [95], DWA algorithms for BP ΔΣ DAC with ternary unit cells [96], DWA and self-calibration algorithms of multi-bit ΔΣ TDC [97], [98].

Here are some comments:

(i) The DWA algorithm with 1st-order noise-shaping of DAC nonlinearities can be implemented with simple hardware, whereas the one for the second-order is complicated; this is valid for all DWA algorithms of the second-order reported up-to now.
(ii) Two DACs are used in a complex BP modulator and its DWA algorithm utilizes cross-coupled order selection of unit cells in two DACs (Fig. 35) [87], [95].
(iii) As far as we know, we are the first for development of the multi-bit ΔΣ TDC DWA algorithm [97], [98].
(iv) To our knowledge, there is no systematic method for development of DWA algorithms [99].
(v) Dynamic matching technique can be also applied to a I, Q-path of a transmitter circuit [100].

## 10. Other Circuits

### 10.1 Folding/Interpolation ADC and Digital Error Correction Algorithm

The author was involved in the development of a high-speed 6-bit ADC using SiGe Hetero-Junction Bipolar Transistor (HBT) for measuring instrument applications [101]. The folding/interpolation architecture is suitable for ADC design with HBT, which employs an analog encoding signal processing.

We also investigated its digital error correction algorithms by finding out very small redundancy [102]. The relationships between error correction and input signal frequency were clarified. The lower bits obtained by the interpolation circuit with redundancy correct the higher bits by the folding circuits.

Later the author realized that this is common for many digital error correction algorithms of various ADCs and that this is similar to a digital adder where lower bits are calculated first and their generated carries are propagated to higher bits.

### 10.2 Background Self-Calibration Algorithm for Pipelined ADC Using Split ADC Scheme

We investigated ADC self-calibration technologies due to the industry demand. The background calibration uses indirect error measurements and an adaptive signal processing algorithm; it is performed during normal operation time. In other words, no calibration time slot is required. All of these operations are done by the circuit itself without help of the circuit user outside.

As one of them we investigated a background calibration algorithm for a pipelined ADC with an open-loop amplifier using a split ADC structure [103]. The open-loop amplifier is employed as a residue amplifier in the first stage of the pipelined ADC to realize low power and high speed (Fig. 40). However, the residue amplifier as well as the DAC suffer from gain error and non-linearity, and hence they need calibration. We investigated the split ADC structure for its background calibration with fast convergence.

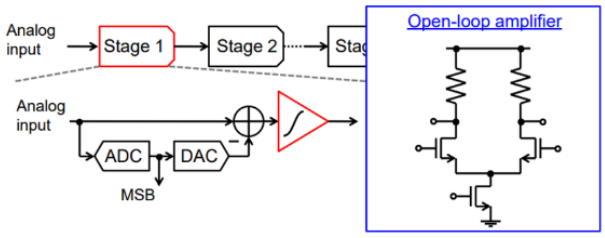



**Fig. 40** Pipeline ADC using open-loop amplifier [103].

### 10.3 Analysis and Design of Operational Amplifier Stability Based on Routh-Hurwitz Stability Criterion

Control theory is basis of analog circuit design. Bode chart based on Nyquist stability criterion is widely used for operational amplifier design. But the author wondered why Routh-Hurwitz stability criterion was not used in circuit design, and finally realized that many of AMS circuit designers did not know it correctly; this fact was very surprising to the author.

Then we investigated to use Routh-Hurwitz stability criterion in addition to Nyquist one for analysis and design of the operational amplifier stability, when its small equivalent circuit is derived; this can lead to explicit stability condition derivation for operational amplifier circuit parameters, and this is effective especially for multi-stage operational amplifiers [104].

### 10.4 MOS Reference Current Source

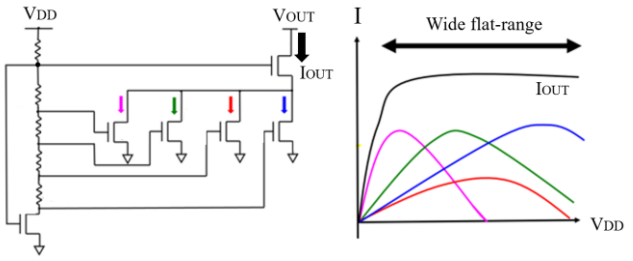
During the author's lecture about CMOS analog circuit to his laboratory members, he assigned several modifications of current sources and one of students showed her simulation results, which was the design improvement of the constant current source (peaking current mirror), originally invented by Nagata Minoru in 1966 (Fig. 41(a)).

Also, several researchers in industry suggested MOS drain current temperature characteristics with respect to the gate voltage (Fig. 41(b)).

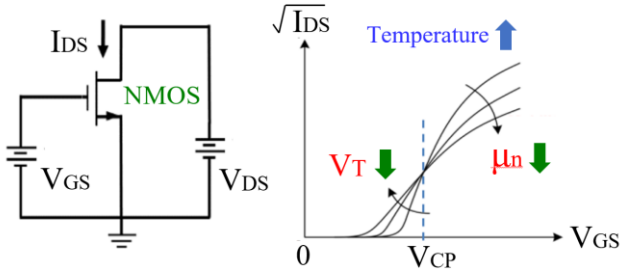
We applied these to MOS reference current source circuits insensitive to supply voltage and temperature [105]–[108]. These demonstrated that there are still analog circuit design challenges with a small number of MOS transistors.

### 10.5 AMS Circuit and System Testing Technologies

AMS circuit and system testing technologies are important but their researchers are not so many in universities. Then we have been engaged in the research for them by collaborating with industry [109]–[124]. These are at the boundary between AMS circuit and LSI testing technologies. Also, Physically Unclonable Function (PUF) has been investigated by applying the TDC linearity self-calibration method [125].




(a) For power supply insensitivity.




(b) For temperature insensitivity.

**Fig. 41** Investigated MOS reference current source [108] ©IEEE.

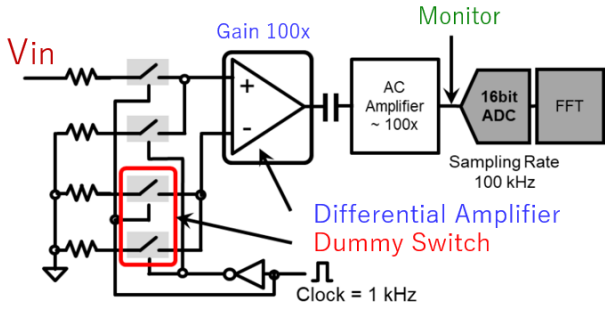



**Fig. 42** DC-AC conversion circuit [124] ©IEEE.

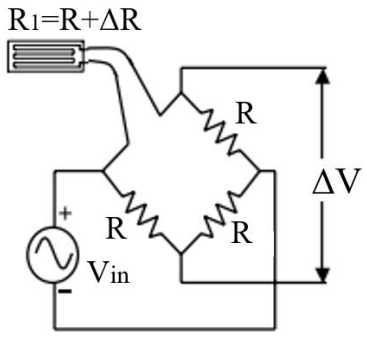



**Fig. 43** Bridge circuit with strain gauge [126].

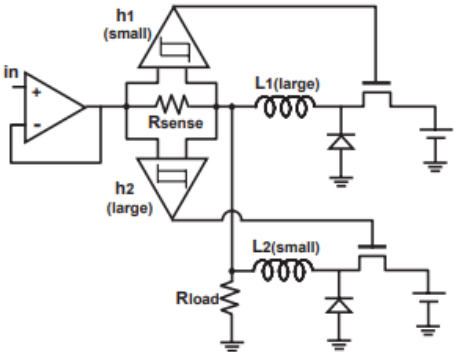



**Fig. 44** Envelope tracking power supply circuit [138] ©IEEE.

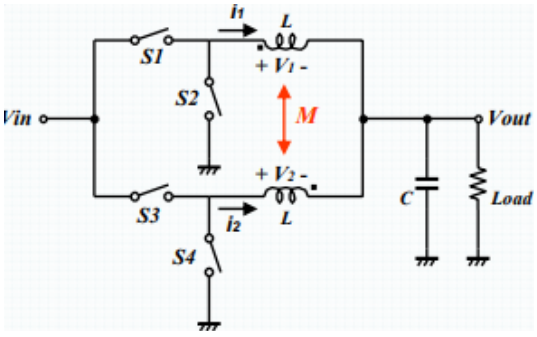



**Fig. 45** Two-phase coupled-inductor buck converter [139].

## 10.6 DC-AC Conversion Technique for Very Small DC Voltage

The author experienced two industry-collaboration research projects with two different companies independently. Both are for very small DC voltage measurement; one is that for analog IC related small voltage/current with DC-AC conversion (Fig. 42) [122]–[124] and the other is that for strain measurement using strain gauge (Fig. 43) [126]. Both research associates used the DC-AC conversion technique and both were successful. We recognized that in general this technique is useful for very small DC voltage measurement with high accuracy by suppressing the low-frequency noise effects.

## 10.7 Power Electronics Circuits

We consider that power electronics circuits play an important role worldwide, and we have been engaged in their study with our research associates: DC-DC converter [127]–[130], EMI reduction [131], [132], charge pump circuit [133]–[135], measurement technique [136], energy harvest [137], envelope tracking power supply (Fig. 44) [138], coupled inductor analysis (Fig. 45) [139], digital PWM generator [140] and IGBT gate driver [141].

## 10.8 Floating-Point Digital Arithmetic Circuit Based on Taylor-Series Expansion

The author realized that Taylor-series expansion has its conversion region; for some functions, it is very wide while for others, it is limited. Then we considered to apply it to some floating-point digital arithmetic circuits for good tradeoff among memory size, required numbers of

additions/subtractions/multiplications, and computing accuracy [142], [143].

### 10.9 Research Results Led by Research Associates

There are also some research results led by visiting professors and researchers as well as Ph.D. course students in the author's lab: device modeling [144]–[147], laterally diffused MOS (LDMOS) device [148]–[150], analog filter [151]–[154], sensor [155], neural network [156], wireless power transmission [157], computer fluid dynamics [158] and distancing-free mask [159], [160].

## 11. Conclusion

This paper has reviewed the author's group research achievements in AMS circuit and system area with the introduction of thinking way and research motivation. Thanks to many excellent research collaborators and students, they cover wide range of areas such as algorithms, circuits, systems, modeling, devices, and testing. Since some of them are algorithm-oriented and technology-independent, hopefully they can live a long time in digital exploding society. This paper is closed by remarking that teaching students at classes as well as discussions with researchers are very helpful for new ideas.

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