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FOREWORD

Special Section on Design Methodologies for System on a Chip

In integrating a giga-scale system on a chip using nano-scale transistors, we are confronted with various issues at each design stage such as design complexity, variation, power concentration, soft-error, and dependability. This series of special sections, the first one of which was published five years ago, provide good opportunities for researchers to publish and learn about their recent leading-edge works on design methodologies for System on a Chip.

For this special section, we have received 14 papers including 1 letter. We made thorough review and the paper selection meeting with all editorial committee members, and finally selected 6 papers including 1 letter.

On behalf of the guest editorial committee, I would like to express our sincere appreciation to all authors of papers submitted to this special section. I would also like to express my thanks to all members of the guest editorial committee and all reviewers for their work on judging the quality of papers. I should thank Professor Hiroshi Tsutsui from Hokkaido University, Professor Yukihide Kohira from the University of Aizu, and Professor Masato Inagi from Hiroshima City University for their work as Guest Editors. Thanks are also due to the IEICE headquarters for the support to this special section.

Kiyoharu Hamaguchi, Guest Editor-in-Chief

Kiyoharu Hamaguchi *(Member)* is a professor at Institute of Science and Engineering, Academic Assembly, Shimane University. His research interests include design synthesis, design verification and computer aided design. He was Technical Program Committee Chair of the 21st Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2018). Hamaguchi has received Doctor of Engineering from Kyoto University.