FOREWORD

Special Section on Optimization and Learning Algorithms of Small Embedded Devices and Related Software/Hardware Implementation

Rapid-growth of embedded system technologies not only in home electric appliances but in industrial equipment is nothing short of eye-opening. And it is quite sure that the growth is comes from performance improvements to microcomputers and programmable devices, which enable remarkable speed-up in learning and optimization algorithms. However, resources for such embedded systems are limited, which forces researchers to reconfigure optimization and learning algorithms to execute in restricted environments. Further improvements to optimization and learning algorithms under software-hardware co-design and co-implementation are thus indispensable for the future embedded systems. This special section was compiled against this background and publishes selected papers related to this subject.

Thirteen papers were submitted not only from Japan but from other countries, and four papers were accepted as the result of careful review process. The accepted papers include some topics from basic machine learning algorithm to hardware implementation of real-world application, each of which is tightly related to the future embedded systems.

We editorial committee members sincerely appreciate the IEICE Information and Systems Society Transaction Editorial Committee for covering our proposed special section and their support for its publication. We hope that this special section will contribute further improvements to the optimization and learning algorithms and embedded devices, and will inspire as many researches to get interested in this field as possible. I am deeply grateful to all the authors, the reviewers, and the editorial committee members for their contributions and efforts for the success of this special section.

Moritoshi Yasunaga, Guest Editor-in-Chief

Moritoshi Yasunaga *(Senior Member)* received the Ph.D. degree in Engineering from the University of Tsukuba in 1994. From 1981 to 1994, he was a researcher of the Central Research Laboratory, Hitachi Ltd., Japan, and he was an invited researcher at the Center for Machine Translation in the Carnegie Mellon University from 1991 to 1992 also. He joined the faculty of the Institute of Information Sciences and Electronics, the University of Tsukuba in 1994. Currently he is a professor in the Graduate School of Systems and Information Engineering in the same university. His research interests include reconfigurable hardware, evolvable hardware, high-speed VLSI design and high-speed signal transmission. He is the recipient of the best paper awards of FPGA conference in 2005, International Conference on Evolvable Systems 2008, and IEICE transactions in 2011. He was the chairperson of Technical Committee on Reconfigurable systems in the IEICE Information System Society, and other chairpersons of various technical committees and international conferences.