FOREWORD

Special Section on Reconfigurable Systems

Reconfigurable Systems are the processing system that can flexibly exploit the parallelism of the algorithm, and run it directly on the processing device. By using the parallelism of the parallel algorithm, Reconfigurable Systems are possible to balance computing performance, processing device size and power consumption, on various positions. With such flexibility, Reconfigurable Systems are adaptable for implementing various systems such as "small embedded systems" to "large-scale supercomputers" efficiently. In addition, the flexibility of Reconfigurable Systems lets us program the internal structure of processing device. With the flexibility in the internal structure of the device, various fault-tolerant designs and also power saving designs are possible in logic-gate level and system level.

However, because of the various aspects of the Reconfigurable Systems the design framework for it requires a wider and a different set of knowledge than on the traditional systems, in the area of application, system software, computer architecture, and device technology. To make the Reconfigurable Systems become a more practical technology in the industry, advanced researches and developments in this area are needed to be presented widely to show what can be done.

So we planned a special section in order to sum up the recent advanced researches and developments of various areas on reconfigurable systems. In response to the call for papers for this special section, 16 regular papers and 4 letter papers were submitted. Through the same review and editorial process as the regular section, 8 papers and 2 letters were accepted for publication. The selected papers will give readers the latest results of researches in various fields of Reconfigurable Systems.

The special section editorial committee members listed below wish to thank all of those who submitted papers, as well as the reviewers for their thoughtful comments and suggestions. As the guest editor, I would wish to convey my earnest thanks to the editorial committee members for their endeavors to preserve the quality of the selected papers high.

The Special Section Editorial Committee Members:
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Tetsuo Hironaka, Guest Editor-in-Chief

Tetsuo Hironaka *(Member)* received the Ph.D. degrees from Kyushu University in 1993. He is now a Professor in the Department of Computer and Network Engineering, Hiroshima City University. His research interests are in the areas of reconfigurable computing architectures and parallel computing.