FOREWORD

Special Section on Parallel and Distributed Computing and Networking

Parallel and distributed computing and networking techniques are increasing their role in realizing enabling technologies in the big-data era. One of the hottest enabling technologies is deep learning, which has significantly improved the quality of object recognition systems by multi-layered neural networks with big training data. Sophisticated neural networks require the best model parameters estimated from enormous data collected through evolving networks. Such an innovation would not have been possible without parallel and distributed computing and networking techniques, which are the main focus of this special issue.

This special section brings together high-quality papers on recent progress in the interdisciplinary area of parallel and distributed computing and networking. These timely papers include the extended versions of conference papers presented at the International Symposium on Computing and Networking (CANDAR'14) and the International Symposium on Embedded Multicore/Many-core System-on-Chip (MCSoC'14), in addition to bland-new contributions from other IEICE members.

A total of 30 papers and 4 letters were submitted from 5 different countries: 19 from Japan, 10 from China, 3 from Taiwan, 1 from each of Brazil and Italy. Each manuscript was carefully reviewed by expert reviewers, and 14 papers and 3 letters were accepted for publication. We had to reject some of the interesting papers, because it is the editorial policy of IEICE transactions to reject a manuscript that requires a major revision. I hope I could see the revised versions of these manuscripts in the future issues of IEICE transactions.

It is my honor to serve as the guest editor-in-chief of this special section. I would like to thank all contributors who submitted their high-quality papers. Also, I wish to express my gratitude to the efforts and contributions of the reviewers and the guest associate editors. Finally, I am most grateful to guest editors, Dr. Ryoichi Shinkuma and Dr. Fumihiko Ino, for their devotion to this special section.

Yasuhiko Nakashima (Nara Institute of Science and Technology), Guest Editor-in-Chief

Yasuhiko NAKASHIMA *(Senior Member)* received B.E., M.E. and Ph.D. degree in Computer Engineering from Kyoto University in 1986, 1988 and 1998 respectively. He was a computer architect in the Computer and System Architecture Department, FUJITSU Limited from 1988 to 1999. From 1999 to 2005, he was an associate professor in Graduate School of Economics, Kyoto University. Since 2006, he has been a professor in the Graduate School of Information Science, Nara Institute of Science and Technology. His research interests include computer architecture, emulation, circuit design, and accelerators. He is a member of IEEE CS, ACM and IPSJ.