IEICE TRANS. INF. & SYST., VOL.E107–D, NO.8 AUGUST 2024

FOREWORD

Special Section on Multiple-Valued Logic and VLSI Computing

Welcome to this Special Section on "Multiple-Valued Logic and VLSI Computing." The papers featured here are primarily extended versions of those presented at the IEEE 53rd International Symposium on Multiple-Valued Logic (ISMVL 2023) held in Matsue, Japan, on May 22–24, 2023. They include substantial additional information beyond the original presentations. We have consistently published special issues in conjunction with ISMVL events in Japan, such as those in Toyama in 2013, Sapporo in 2016, and Miyazaki in 2020. The aim of this Special Section is to provide an overview of recent research advancements in various aspects related to multiple-valued concepts to the many readers of this transaction who are interested in innovative, new-concept VLSI computing and its applications.

The nine contributing papers span a broad range, including logic design, VLSI architecture, communication for VLSI, quantum computing design, and innovative applications such as reversible logic and neural networks. We extend our gratitude to all the authors who contributed papers and the reviewers who worked diligently to ensure that the papers were of publication quality. We hope that this special section will foster further discussions among readers on the interdisciplinary fields of multiple-valued logic and VLSI computing.

Yasushi Yuminaka (Gunma Univ.), Guest Editor-in-Chief

Yasushi Yuminaka *(Senior Member)* received B. E., M. E., and D. E. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1990, 1992, and 1995, respectively. He is currently a Professor in the Division of Electronics and Informatics, Graduate School of Science and Technology, Gunma University, Kiryu, Japan. His research interests include the design of multiple-valued integrated circuits, high-speed interfaces for VLSI systems, and new-paradigm computing systems and their applications. Dr. Yuminaka received the IEE Ambrose Fleming Premium Award in 1994, the Niwa Memorial Award in 1995, the Young Engineer Award from the IEICE of Japan in 1995, and the Outstanding Contributed Paper Award at the IEEE International Symposium on Multiple-Valued Logic in 2000 and 2009. He served as a Program Chair for IEEE International Symposium on Multiple-Valued Logic in 2013, 2016, and 2020, and a Symposium Chair for IEEE International Symposium on Multiple-Valued Logic in 2023. He was a Chair (2020–2021) of the IEEE Computer Society Technical Committee on Multiple-Valued Logic. He is senior members of IEEE and IEEJ.