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FOREWORD

Special Section on Test and Verification of VLSIs

The Fifteenth Asian Test Symposium (ATS'06) and the Seventh Workshop on RTL and High Level Testing (WRTLT'06) were held in Fukuoka, Japan on November 20th–23rd and 23rd–24th, respectively. Excellent works on state-of-the-art and wide-spread ideas and techniques were presented and discussed in ATS'06, while WRTLT'06 provided more frank discussion focusing on RTL and high level testing. We took these opportunities to promote and encourage researches on VLSI testing and verification more, and planed this special section.

We had 30 submissions including 27 full papers and 3 letters, and the Editorial Committee selected 16 full papers and 2 letters for publication through careful reviews. The accepted works cover Fault Detection, Fault Diagnosis, Verification, Test Compaction, Processor Testing, SoC Testing, Secure Test, and Built-In Self-Test.

The Guest Editors would like to appreciate all the authors for their submissions, and the reviewers for their professional and voluntary works. Finally, we would like to express our appreciation to the Editorial Committee Members for devoting a considerable amount of time to the editorial processes. Their names and affiliations are listed below.

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Seiji Kajihara *(Member)* received the B.S. and M.S. degrees from Hiroshima University, Japan, and the Ph.D. degree from Osaka University, Japan,in 1987, 1989, and 1992, respectively. From 1992 to 1995, he worked with the Department of Applied Physics, Osaka University, as an Assistant Professor. In 1996, he joined the Department of Computer Science and Electronics of Kyushu Institute of Technology, Japan, where he is a Professor currently. His research interest includes test generation, delay testing, and design for testability. He received the Young Engineer Award from IEICE in 1997, the Yamashita SIG Research Award from IPSJ in 2002, and the Best Paper Award from IEICE in 2005. Dr. Kajihara is a member of the IEEE and the IPSJ.

Michiko Inoue *(Member)* received her B.E., M.E, and Ph.D. degrees in computer science from Osaka University in 1987, 1989, and 1995 respectively. She worked at Fujitsu Laboratories Ltd. from 1989 to 1991. She is an associate professor of Graduate School of Information Science, Nara institute of Science and Technology (NAIST). Her research interests include distributed algorithms, parallel algorithms, graph theory and design and test of digital systems. She is a member of IEEE, the Information Processing Society of Japan, and Japanese Society for Artificial Intelligence.